CLAIMS

What is claimed is:

1. A method of forming an emitter in a bipolar transistor, comprising:

forming a collector region in a substrate;

forming a base layer over at least a portion of the collector region;

forming a first oxide layer over the base layer;

forming a carbide layer over the first oxide layer;

forming a second oxide layer over the carbide layer;

selectively etching portions of the first and second oxide layers and the carbide layer to expose a portion of the base layer;

depositing a polysilicon emitter layer over the exposed portion of the base layer; and

doping at least a portion of the polysilicon emitter layer.

2. The method of claim 1, wherein forming the first oxide layer comprises:

growing a thermal silicon oxide layer over the base layer, the thermal silicon oxide layer having a thickness of about 20 Å or more and about 50 Å or less; and

depositing a first silicon oxide over the thermal silicon oxide layer to a thickness of about 50 Å using a plasma enhanced chemical vapor deposition process.

3. The method of claim 1, wherein forming the first oxide layer comprises depositing a first silicon oxide over the base layer, the first silicon oxide having a thickness of about 70 Å or more and about 100 Å or less.

4. The method of claim 3, wherein forming the carbide layer comprises depositing a silicon carbide layer over the first oxide layer.

5. The method of claim 4, wherein depositing a silicon carbide layer comprises depositing silicon carbide over the first oxide layer to a thickness of about 100 Å using a plasma enhanced chemical vapor deposition process.

6. The method of claim 4, wherein forming the second oxide layer comprises depositing a second silicon oxide over the carbide layer to a thickness of about 500 Å or more and about 1000 Å or less.

7. The method of claim 6, wherein depositing the second silicon oxide comprises depositing the second silicon oxide over the carbide layer to a thickness of about 500 Å or more and about 1000 Å or less using a plasma enhanced chemical vapor deposition process.

8. The method of claim 3, wherein forming the second oxide layer comprises depositing a second silicon oxide over the carbide layer to a thickness of about 500 Å.

9. The method of claim 1, wherein forming the second oxide layer comprises depositing a second silicon oxide over the carbide layer to a thickness of about 500 Å or more and about 1000 Å or less.

10. The method of claim 1, wherein forming the carbide layer comprises depositing a silicon carbide layer over the first oxide layer.

11. The method of claim 10, wherein depositing a silicon carbide layer comprises depositing silicon carbide over the first oxide layer to a thickness of about 100 Å.

12. The method of claim 7, wherein selectively etching portions of the first and second oxide layers and the carbide layer to expose a portion of the base layer comprises:

etching a portion of the second oxide layer to expose a portion of the carbide layer using a first reactive ion etch process;

etching a portion of the carbide layer to expose a portion of the first oxide layer using a second reactive ion etch process; and

etching a portion of the first oxide layer to expose the portion of the base layer using a wet etch process.

13. The method of claim 1, wherein selectively etching portions of the first and second oxide layers and the carbide layer to expose a portion of the base layer comprises:

etching a portion of the second oxide layer to expose a portion of the carbide layer using a first reactive ion etch process;

etching a portion of the carbide layer to expose a portion of the first oxide layer using a second reactive ion etch process; and

etching a portion of the first oxide layer to expose the portion of the base layer using a wet etch process.

14. The method of claim 13, wherein etching a portion of the second oxide layer comprises:

forming a mask over the second oxide layer, the mask having an opening exposing a portion of the second oxide layer; and

etching an exposed portion of the second oxide layer using a first reactive ion etch process having an etch selectivity to the second oxide layer over the carbide layer greater than about 10:1 to expose a portion of the carbide layer.

15. The method of claim 14, wherein etching a portion of the carbide layer comprises etching an exposed portion of the carbide layer using a second reactive ion etch process having an etch selectivity to the carbide layer over the first oxide layer greater than about 10:1 to expose a portion of the first oxide layer.

16. The method of claim 13, wherein etching a portion of the carbide layer comprises etching an exposed portion of the carbide layer using a second reactive ion etch process having an etch selectivity to the carbide layer over the first oxide layer greater than about 10:1 to expose a portion of the first oxide layer.

17. The method of claim 16, wherein etching a portion of the carbide layer comprises etching an exposed portion of the carbide layer using a second reactive ion etch process having an etch selectivity to the carbide layer over the first oxide layer greater than about 20:1 to expose a portion of the first oxide layer.

18. The method of claim 1, wherein forming the carbide layer comprises depositing one of silicon carbide and boron carbide over the first oxide layer.

19. The method of claim 1, wherein forming the carbide layer comprises depositing a combination of silicon carbide and boron carbide over the first oxide layer.

20. A method of forming an emitter-base dielectric stack in a poly emitter bipolar transistor, comprising:

forming a first oxide layer over a base layer;

forming a carbide layer over the first oxide layer;

forming a second oxide layer over the carbide layer;

selectively etching portions of the first and second oxide layers and the carbide layer to expose a portion of the base layer; and

forming a polysilicon emitter structure over the second oxide layer and the exposed portion of the base layer.

21. The method of claim 20, wherein forming the carbide layer comprises depositing a silicon carbide layer over the first oxide layer.

22. The method of claim 21, wherein depositing a silicon carbide layer comprises depositing silicon carbide over the first oxide layer to a thickness of about 100 Å.

23. The method of claim 20, wherein forming the first oxide layer comprises:

growing a thermal silicon oxide layer over the base layer, the thermal silicon oxide layer having a thickness of about 20 Å or more and about 50 Å or less; and

depositing a first silicon oxide over the thermal silicon oxide layer, the first silicon oxide having a thickness of about 50 Å.

24. The method of claim 23, wherein forming the first oxide layer comprises depositing a first silicon oxide over the base layer, the first silicon oxide having a thickness of about 70 Å or more and about 100 Å or less.

25. The method of claim 20, wherein selectively etching portions of the first and second oxide layers and the carbide layer to expose a portion of the base layer comprises:

etching a portion of the second oxide layer to expose a portion of the carbide layer using a first reactive ion etch process;

etching a portion of the carbide layer to expose a portion of the first oxide layer using a second reactive ion etch process; and

etching a portion of the first oxide layer to expose the portion of the base layer using a wet etch process.

26. The method of claim 25, wherein etching a portion of the second oxide layer comprises:

forming a mask over the second oxide layer, the mask having an opening exposing a portion of the second oxide layer; and

etching an exposed portion of the second oxide layer using a first reactive ion etch process having an etch selectivity to the second oxide layer over the carbide layer greater than about 10:1 to expose a portion of the carbide layer.

27. The method of claim 26, wherein etching a portion of the carbide layer comprises:

etching an exposed portion of the carbide layer using a second reactive ion etch process having an etch selectivity to the carbide layer over the first oxide layer greater than about 10:1 to expose a portion of the first oxide layer; and

stopping on the first oxide layer.

28. The method of claim 25, wherein etching a portion of the carbide layer comprises etching an exposed portion of the carbide layer using a second reactive ion etch process having an etch selectivity to the carbide layer over the first oxide layer greater than about 10:1 to expose a portion of the first oxide layer.

29. The method of claim 28, wherein etching a portion of the carbide layer comprises etching an exposed portion of the carbide layer using a second reactive ion etch process having an etch selectivity to the carbide layer over the first oxide layer greater than about 20:1 to expose a portion of the first oxide layer.

30 The method of claim 20, wherein forming the carbide layer comprises depositing one of silicon carbide and boron carbide over the first oxide layer.

31. A method of forming an emitter in a bipolar transistor, comprising:

forming a collector region in a substrate;

forming a base layer over at least a portion of the collector region;

forming an oxide layer over the base layer;

forming a carbide layer over the oxide layer;

selectively etching portions of the oxide and carbide layers to expose a portion of the base layer;

depositing a polysilicon emitter layer over the exposed portion of the base layer; and

doping at least a portion of the polysilicon emitter layer.

32. The method of claim 31, wherein forming the carbide layer comprises depositing one of silicon carbide and boron carbide over the oxide layer.

33. A bipolar transistor, comprising:

a collector region;

a base region formed in a base layer overlying the collector region;

an emitter-base dielectric stack overlying the base layer and having an opening therein exposing a portion of the base layer, the emitter-base dielectric stack comprising a carbide layer; and

an emitter poly layer overlying the emitter-base dielectric stack and an exposed portion of the base layer.

34. The transistor of claim 33, wherein the emitter-base dielectric stack comprises:

a first oxide layer overlying the base region of the base layer;

a carbide layer overlying the first oxide layer; and

a second oxide layer overlying the carbide layer.

35. The transistor of claim 34, wherein the first oxide layer comprises:

a thermal silicon oxide layer overlying the base layer and having a thickness of about 20 Å or more and about 50 Å or less; and

a first silicon oxide overlying the thermal silicon oxide layer and having a thickness of about 50 Å.

36. The transistor of claim 34, wherein the first oxide layer comprises a first silicon oxide overlying the base layer and having a thickness of about 70 Å or more and about 100 Å or less.

37. The transistor of claim 34, wherein the carbide layer comprises a silicon carbide layer overlying the first oxide layer.

38. The transistor of claim 37, wherein the silicon carbide layer comprises a thickness of about 100 Å.

39. The transistor of claim 37, wherein the second oxide layer comprises a second silicon oxide overlying the carbide layer and having a thickness of about 500 Å or more and about 1000 Å or less.